CLAIMS.

There is claimed:

1. A method for detecting unstable clock-domain crossings in a design of an integrated circuit (IC), comprising:

determining clock-domain crossings in the design;

for each of the determined crossings lacking a structural synchronization cell:

making a stability determination for the crossing, and

giving an indication when the stability determination for the crossing indicates an unstable crossing.

2. The method of claim 1, further comprising highlighting the unstable crossing.

3. The method of claim 1, wherein the crossing includes registers connected to a combinational path, and each of the registers is clocked by a different respective clock signal.

4. The method of claim 3, wherein the register comprises at least one of: a logic flip-flop, a memory cell, and combinational logic loops defining a de-facto memory.

5. The method of claim 3, wherein the combinational path comprises at least one of: a logical AND function, a logical OR function, a logical NAND function, a logical NOR function, a logical NOT function, a logical XOR function, and a multiplexer.

6. The method of claim 1, wherein the structural synchronization cell comprises at least one of a double-level register, a recirculation MUX with double-registered control, and a user defined synchronization cell.

7. The method of claim 1, wherein the stability determination is made based on satisfaction of a stability function.

8. The method of claim 7, wherein the stability function determines whether a first register and a second register change data simultaneously.

9. The method of claim 8, wherein the stability function is dissatisfied when the first register and the second register change data simultaneously.

10. The method of claim 9, wherein the first register belongs to a first clock domain and the second register belongs to a second clock domain, and the first and second clock domains are part of the crossing.

11. The method of claim 1, wherein the stability determination is performed using at least one of model checking and bounded model checking (BMC).

12. The method of claim 1, wherein the unstable crossing is indicated when a time frame destabilizes the crossing.

13. The method of claim 12, wherein the time frame comprises a set of clock signals, and wherein each of the clock signals clock a different register belonging to the crossing.

14. The method of claim 1, further comprising using a clock synchronization analysis tool to identify candidate unstable crossings, wherein the candidate unstable crossings are each verified by making a respective stability determination for the candidate crossing, and eliminating a candidate unstable crossing when the

stability determination for the candidate unstable crossing does not indicate an unstable crossing.

15. The method of claim 1, executed on at least one of: computer aided design (CAD) system, a CAD program, a clock synchronization analysis tool.

16. A computer program product, including a computer readable medium with computer instructions, for use by a computer to perform operations for detecting unstable clock-domain crossings in a design of an integrated circuit (IC), the operations comprising:

determining clock-domain crossings in the design;

for each of the determined crossings lacking a structural synchronization cell:

making a stability determination for the crossing, and

giving an indication when the stability determination for the crossing indicates an unstable crossing.

17. The computer program product of claim 16, wherein the operations further comprise highlighting the unstable crossing.

18. The computer program product of claim 16, wherein the crossing includes registers connected to a combinational path, and each of the registers is clocked by a different respective clock signal.

19. The computer program product of claim 18, wherein the register comprises at least one of: a logic flip-flop, a memory cell, and combinational logic loops defining a de-facto memory.

20. The computer program product of claim 18, wherein the combinational path comprises at least one of: a logical AND function, a logical OR function, a logical NAND function, a logical NOR function, a logical NOT function, a logical XOR function, and a multiplexer.

21. The computer program product of claim 16, wherein the structural synchronization cell comprises at least one of a double-level register, a recirculation MUX with double-registered control, and a user defined synchronization cell.

22. The computer program product of claim 16, wherein the stability determination is made based on satisfaction of a stability function.

23. The computer program product of claim 22, wherein the stability function determines whether a first register and a second register change data simultaneously.

24. The computer program product of claim 23, wherein the stability function is dissatisfied when the first register and the second register change data simultaneously.

25. The computer program product of claim 24, wherein the first register belongs to a first clock domain and the second register belongs to a second clock domain, and the first and second clock domains are part of the crossing.

26. The computer program product of claim 16, wherein the stability determination is performed using at least one of model checking and bounded model checking.

27. The computer program product of claim 16, wherein the unstable crossing is indicated when a time frame destabilizes the crossing.

28. The computer program product of claim 27, wherein the time frame comprises a set of clock signals, and wherein each of the clock signals clock a different register belonging to the crossing.

29. The computer program product of claim 16, further comprising using a clock synchronization analysis tool to identify candidate unstable crossings, wherein the candidate unstable crossings are each verified by making a respective stability determination for the candidate crossing, and eliminating a candidate unstable crossing when the stability determination for the candidate unstable crossing does not indicate an unstable crossing.

30. The computer program product of claim 16, executed on at least one of: computer aided design (CAD) system, a CAD program, a clock synchronization analysis tool.

31. A computer system, adapted to implement a method for detecting unstable clock-domain crossings in a design of an integrated circuit (IC), comprising:

a processor; and,

a memory including software instructions adapted to enable the computer system to perform the operations of:

determining clock-domain crossings in the design;

for each of the determined crossings lacking a structural synchronization cell:

making a stability determination for the crossing, and

giving an indication when the stability determination for the crossing indicates an unstable crossing.

32. The computer system of claim 31, wherein the operations further comprise highlighting the unstable crossing.

33. The computer system of claim 31, wherein the crossing includes registers connected to a combinational path, and each of the registers is clocked by a different respective clock signal.

34. The computer system of claim 33, wherein the register comprises at least one of: a logic flip-flop, a memory cell, and combinational logic loops defining a de-facto memory.

35. The computer system of claim 33, wherein the combinational path comprises at least one of: a logical AND function, a logical OR function, a logical NAND function, a logical NOR function, a logical NOT function, a logical XOR function, and a multiplexer.

36. The computer system of claim 31, wherein the structural synchronization cell comprises at least one of a double-level register, a recirculation MUX with double-registered control, and a user defined synchronization cell.

37. The computer system of claim 31, wherein the stability determination is made based on satisfaction of a stability function.

38. The computer system of claim 37, wherein the stability function determines whether a first register and a second register change data simultaneously.

39. The computer system of claim 38, wherein the stability function is dissatisfied when the first register and the second register change data simultaneously.

40. The computer system of claim 39, wherein the first register belongs to a first clock domain and the second register belongs to a second clock domain, and the first and second clock domains are part of the crossing.

41. The computer system of claim 31, wherein the stability determination is performed using at least one of model checking and bounded model checking (BMC).

42. The computer system of claim 31, wherein the unstable crossing is indicated when a time frame destabilizes the crossing.

43. The computer system of claim 42, wherein the time frame comprises a set of clock signals, and wherein each of the clock signals clock a different register belonging to the crossing.

44. The computer system of claim 31, further comprising using a clock synchronization analysis tool to identify candidate unstable crossings, wherein the candidate unstable crossings are each verified by making a respective stability determination for the candidate crossing, and eliminating a candidate unstable crossing when the

stability determination for the candidate unstable crossing does not indicate an unstable crossing.

45. The computer system of claim 31, wherein the operations are executed in connection with one of a computer aided design (CAD) system, a CAD program, and a clock synchronization analysis tool.